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(71) Applicant: FAIRCHILD SEMICONDUCTOR CORPORATION [US/US]; 333 Western Avenue, South Portland, ME 04106 (US).

(72) Inventor: JOSHI, Rajeev; 10168 Colby Avenue, Cupertino, CA 95014 (US).

(74) Agents: SANI, Babak, S. et al.; Townsend and Townsend and Crew LLP, 8th Floor, Two Embarcadero Center, San Francisco, CA 94111-3834 (US).

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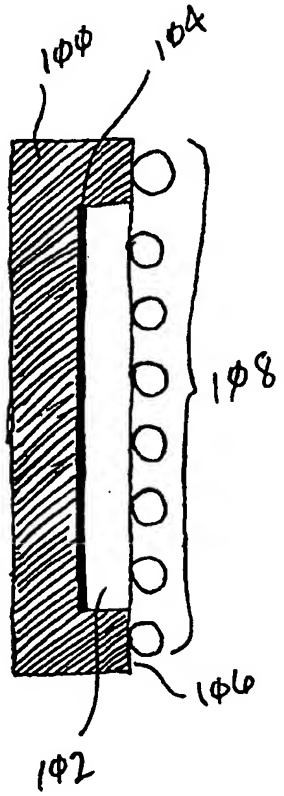
(54) Title: HIGH PERFORMANCE FLIP CHIP PACKAGE

(57) Abstract

An improved semiconductor package that reduces package resistance to a negligible level, and offers superior thermal performance. A silicon die (102) is attached to a carrier (100) (or substrate) that has a cavity surrounding the die (102). Direct connection of the active surface of the silicon die (102) to the printed circuit board is then made by an array of solder bumps (108) that is distributed across the surface of the die (102) as well as the edges of the carrier (100) surrounding the die (102).



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HIGH PERFORMANCE FLIP CHIP PACKAGE

BACKGROUND OF THE INVENTION

The present invention relates in general to semiconductor packaging and in particular to an apparatus and method of manufacture for a high performance flip chip package for semiconductor devices.

While silicon process technology has advanced significantly in the past decade, for the most part, the same decades-old package technology continues as the primary packaging means. Epoxy or solder die attach along with aluminum or gold wire bonding to lead frame is still the preferred semiconductor package methodology. Advances in semiconductor processing technology, however, have made the parasitics associated with conventional packages more of a performance limiting factor. This is particularly true in the case of power switching devices where, as in the case of power MOSFETs, the on-resistance of these devices continues to push the lower limits. Thus, the parasitic resistance introduced by the bond wires and the lead frame in conventional packages becomes much more significant for such high current devices as power MOSFETs. Furthermore, the continuous shrinking of geometries and the resulting increase in chip densities has given rise to an increasing demand for semiconductor packages with lead counts higher than that offered by the conventional packaging techniques.

Ball grid array and flip chip technologies were developed to address some of these demands. Both of these packaging technologies provide for a more direct connection between the silicon die and the printed circuit board as well as providing for higher interconnect densities. There is always room for

improvement however. For example, a typical ball grid array package consists of a BT resin laminated board which serves as an interposer layer between the silicon die and the printed circuit board (PCB). Because of poor heat dissipation from the laminated board, external heat sinks and additional PCB copper layers are often required to dissipate excess heat.

In the case of conventional flip chip technology, among other shortcomings, heat dissipation is essentially governed by the die size and connection to the back side of the die is not easily facilitated (often requiring a bond wire connection). These limitations (poor heat dissipation and resistive contact to back side) become quite significant in high current applications such as power switching devices. A substantial improvement in the performance of flip chip packages is offered by Bencuya et al. in commonly assigned provisional Patent Application Number _____, (Attorney Docket No. 018865-0006) entitled "Low Resistance Package for Semiconductor Devices." In one embodiment, this improved package eliminates wire bonding by making direct connection between an array of solder balls on one conductive surface of the die and a lead frame element, while connection to the opposite side is made by a die attached mechanism. This package exhibits significantly lower resistance; however, it still relies on a lead frame which adds residual resistance to the current path, and is not the smallest package possible for a given die size.

There is therefore a need for a high density semiconductor package whose attributes are minimal parasitic resistance and good heat dissipation, and that is readily manufacturable.

SUMMARY OF THE INVENTION

The present invention provides an improved semiconductor package that reduces package resistance to a negligible level, and offers superior thermal performance. Broadly, according to the present invention, a silicon die is attached to a carrier (or substrate) that has a cavity substantially surrounding the

die. Direct connection of the active surface of the silicon die to the printed circuit board is then made by an array of solder bumps that is distributed across the surface of the die as well as the edges of the carrier surrounding the die. In one embodiment, the outer array of solder balls connects to a conductive carrier and provides for a low resistance connection to the back side of the die. In applications where no connection to the back side of the die is required, the carrier and the array of solder balls connecting to it may act as a thermal via for dissipating heat. Alternatively, the carrier may be of dielectric material with selective conductive traces to make selective contact to traces on the board through the outer array of solder balls. The package of the present invention also reduces the number of steps required in the assembly process flow and is manufactured using standard materials and equipment. The resulting package not only exhibits minimal resistance and improved heat dissipation, it is very thin and light as well as being cost-effective to manufacture.

Accordingly, in one embodiment, the present invention provides a semiconductor package including a carrier having a cavity sized for housing a silicon die, a silicon die having a first surface attached to the inside of the cavity, the silicon die having a thickness substantially equal to a depth of the cavity such that a second surface of the silicon die and a surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane, and an array of solder balls distributed across the uniform plane connecting to the second surface of the silicon die as well as the surface of the edges of the carrier surrounding the silicon die.

In another embodiment, the present invention provides a method of packaging a silicon die including the steps of: stamping a cavity in a carrier for housing the silicon die; attaching a first surface of the silicon die inside the cavity such that a second surface of the silicon die and a surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane; and disposing an array of solder balls across the substantially uniform plane with an

outer array connecting to the carrier and an inner array connecting to the second surface of the silicon die.

A better understanding of the nature and advantages of the improved flip chip package of the present invention may be gained with reference to the detailed description and drawings below.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a side view of the improved flip chip package according to the present invention;

Figure 2 illustrates the flip chip package of the present invention showing the active surface of the package with an array of solder balls;

Figure 3 shows the printed circuit board side with exemplary traces for receiving the flip chip package of the present invention; and

Figure 4 shows an exemplary embodiment for a carrier panel with multiple carriers that may be used during the process flow of the flip chip package of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figure 1, there is shown a side view of the improved flip chip package according to the present invention. A carrier 100 is provided with a rectangular cavity to receive the silicon die. A silicon wafer that has been previously back lapped and metallized to product specifications is diced and a die 102 is attached inside the cavity using any one of a variety of well known die attach methods including conductive epoxy, or soft or hard solder connection. The cavity dimensions are designed such that the cavity depth is substantially equal to the thickness of die 102 plus the thickness of die attach bond line 104. This ensures that the outer surface of die 102 and the edge surface 106 of carrier

100 surrounding die 102 form a uniform plane. Solder paste is dispensed on the surface of die 102 as well as the carrier edge surface 106. The solder paste is then reflowed using conventional methodology to form solder balls 108. Alternatively, either die 102 or carrier surfaces 106, or both can be already solder bumped prior to the die attach step. Finally, the edges of die 102 may be sealed using, for example, a conventional liquid glob top epoxy. This results in a highly compact package that is light and thin. A typical silicon die may be, for example, 0.008 inches thick and the thickness of carrier 100 at the bottom of the cavity may be, for example, 0.008 inches. This results in an exemplary package that is only 0.4 millimeter in thickness (and about 0.6 millimeter with solder balls).

The flip chip package of the present invention is particularly well suited for discrete products with high heat dissipation such as power switching devices (e.g., power MOSFETs) where electrical connection to the back side of the die (MOSFET drain terminal) is required. By using conductive material such as copper for carrier 100, the package of the present invention provides for a very low resistance, compact connection between the back side of the die (the drain terminal of the power MOSFET) and the PCB. Figure 2 is a top view of the active surface of the package of the present invention showing the array of solder balls 108. The same reference numerals denote identical elements in all of the Figures. Solder ball array 108 is divided into two groups, a first outer array of solder balls 108-1 that connects to carrier edge surface 106 and an internal array of solder balls 108-2 connecting to the die surface. When housing a power MOSFET, solder balls 108-1 provide the connection to the drain terminal, and solder balls 108-2 provide the connection to the source and gate terminals. In the embodiment shown in Figure 2, a corner solder ball 108-2G is dedicated for the gate terminal and the remaining solder balls in array 108-2 provide for a distributed, low resistance connection to the source terminal of the MOSFET. The combination of a highly conductive carrier 100 and array of solder balls 108-1 plus a distributed array of solder balls 108-2 across the surface

of the die virtually eliminate the metal resistance by drastically reducing the length of the current path through the metal connections. Figure 3 shows the printed circuit board side with exemplary traces for receiving the flip chip package shown in Figure 2.

It is to be understood that a conductive carrier for power MOSFET applications is used herein for illustrative purposes only, and that carrier 100 may be made of dielectric material such as ceramic for various other applications. Selective contact to the back side of the die is still possible with selective conductive traces through the ceramic carrier. In cases where no contact to the back side of the die is required, a metal carrier that makes no electrical contact to the die can still be used along with solder ball array 108-1 (that may be shorted together) to form a thermal via. This provides a very efficient mechanism for dissipating heat.

Another significant advantage of the improved flip chip package of the present invention is that it not only does not introduce any steps that deviate from industry standard practices, it eliminates various steps and simplifies the process of manufacture. Because the process of manufacture for the package of the present invention follows existing standards in the industry (e.g., fine pitch ball grid array standards), the tools and infrastructure necessary to support the package such as sockets, handlers, trays and the like are well established. In terms of simplification of the process of manufacture, the entire assembly process flow for the package of the present invention is reduced to the following steps: 1) wafer saw; 2) die attach and solder ball attach; 3) third optical; 4) encapsulate; 5) test; 6) singulate; and 7) tape and reel. This eliminates the need for costly mold, trim and form equipment and a plating line. Other ball count variations of the package can be easily tooled up with an initial investment in a carrier rather than dedicated items like mold, trim and form tooling that are needed for conventional surface mount packages. This improves time to market for new form factor packages.

Due to its relatively simple structure, a panel of carriers that receives the silicon dies is less costly compared to lead frames with intricate traces as required by conventional packaging. An exemplary panel 400 of carriers is shown in Figure 4. Panel 400 is made of the carrier material (e.g., copper or ceramic depending on the application) with an array of identical cavities 402 stamped across its surface the dimensions of which are governed by that of the die they will house. In one embodiment, panel 400 may include the outer array of solder balls (108-1 in Figure 2) already attached around each cavity 402 as shown. Alternatively, solder balls (108-1) may be attached later during the assembly process flow. The carriers may be tested while in a panel form and marked. The units are then individually singulated by sawing and shipped using conventional packing methods.

Thus, the present invention provides a high performance flip chip type package that offers a number of advantages over existing packaging techniques. The combination of a die attached inside a cavity of a carrier such that an array of solder balls can be disposed across both surfaces results in a highly compact, low resistance package with a simplified and thus cost effective method manufacture. The package also improves heat dissipation when the carrier is made of a highly conductive material acting as a thermal via. While the above is a complete description of the preferred embodiment of the present invention, it is possible to use various alternatives, modifications and equivalents. Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claims, along with their full scope of equivalents.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a carrier having a cavity sized for housing a silicon die;

a silicon die having a first surface attached to the inside of the cavity, the silicon die having a thickness substantially equal to a depth of the cavity such that a second surface of the silicon die and a surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane; and

an array of solder balls distributed across the uniform plane and divided into an inner array connecting to the second surface of the silicon die an outer array connecting to the surface of the edges of the carrier surrounding the silicon die.

2. The semiconductor package of claim 1 wherein the carrier is made of electrically conductive material.

3. The semiconductor package of claim 2 wherein the carrier makes electrical contact with the first surface of the silicon die.

4. The semiconductor package of claim 3 wherein the silicon die comprises a power MOSFET having a drain terminal, a source terminal, and a gate terminal.

5. The semiconductor package of claim 4 wherein the drain terminal of the power MOSFET connects to the carrier and the outer array of solder balls, the source terminal of the power MOSFET connects to a substantial number of the inner array of solder balls, and the gate terminal of the power MOSFET connects to one of the inner array of solder balls.

6. The semiconductor package of claim 2 wherein the carrier and the outer array of solder balls are configured to act as a thermal via.

7. The semiconductor package of claim 1 wherein the carrier is made of dielectric material.

8. A method for packaging a silicon die comprising the steps of:

stamping a cavity in a carrier for housing the silicon die;

attaching a first surface of the silicon die inside the cavity such that a second surface of the silicon die and a surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane; and

disposing an array of solder balls across the substantially uniform plane with an outer array connecting to the carrier and an inner array connecting to the second surface of the silicon die.

9. The method for packaging a silicon die as in claim 8 wherein said carrier is in a panel form and said step of stamping stamps a plurality of cavities across the panel.

10. The method for packaging a silicon die as in claim 9 further comprising the step of singulating the panel into plural units.

11. The method for packaging a silicon die as in claim 8 wherein the step of disposing an array of solder balls occurs prior to the attaching step and comprises a step of forming solder balls on the second surface of the silicon die, and a step of forming solder balls on the surface of the edges of the carrier.

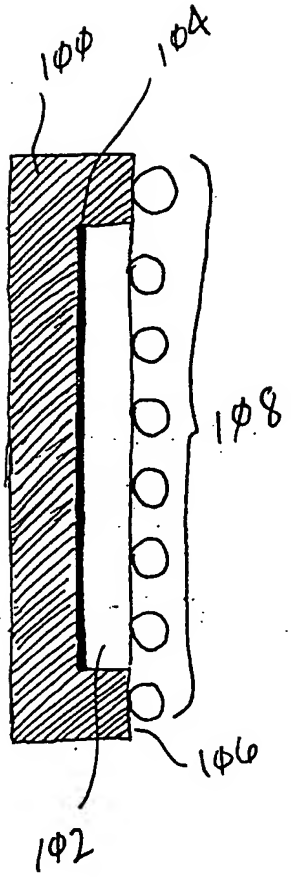
12. A package for a silicon die comprising a power MOSFET with a source terminal, a drain terminal and a gate terminal, the package comprising:

a conductive carrier having a cavity sized for housing the silicon die such that when the silicon die is attached to the inside of the cavity an outer surface of the silicon die and the surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane;

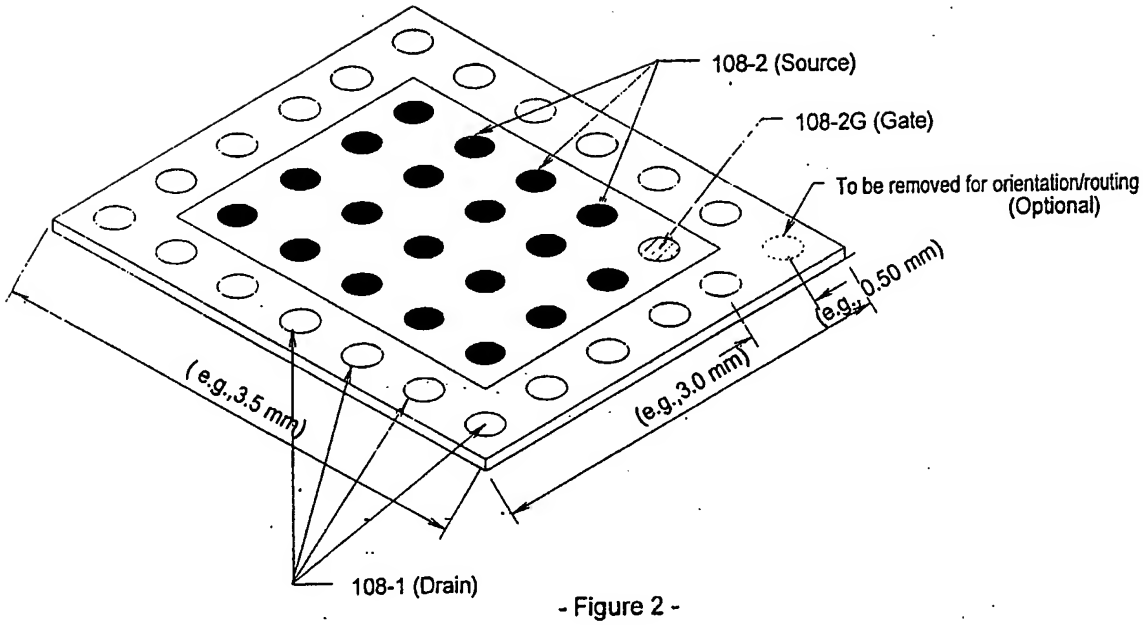
a first array of solder balls disposed across the outer surface of the silicon and making contact to the source terminal of the power MOSFET; and

a second array of solder balls disposed across the surface of the edges of the carrier surrounding the silicon die and making contact to the drain terminal of the power MOSFET through the conductive carrier.

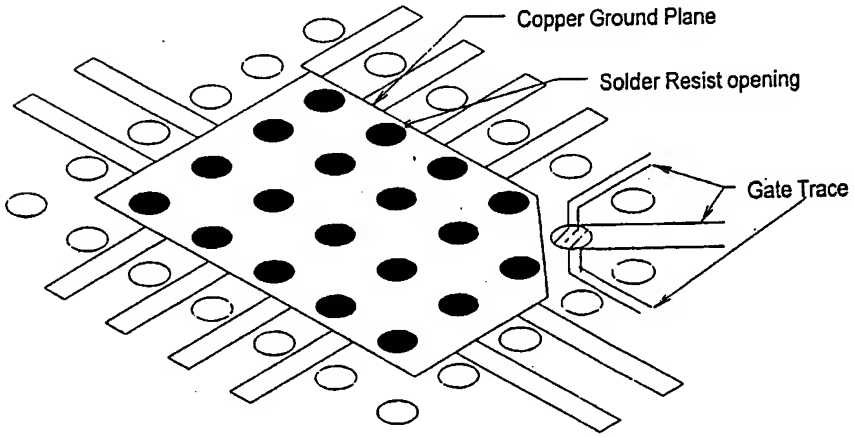
13. The package of claim 12 wherein a solder ball on the outer surface of the silicon die makes contact to the gate terminal of the power MOSFET.



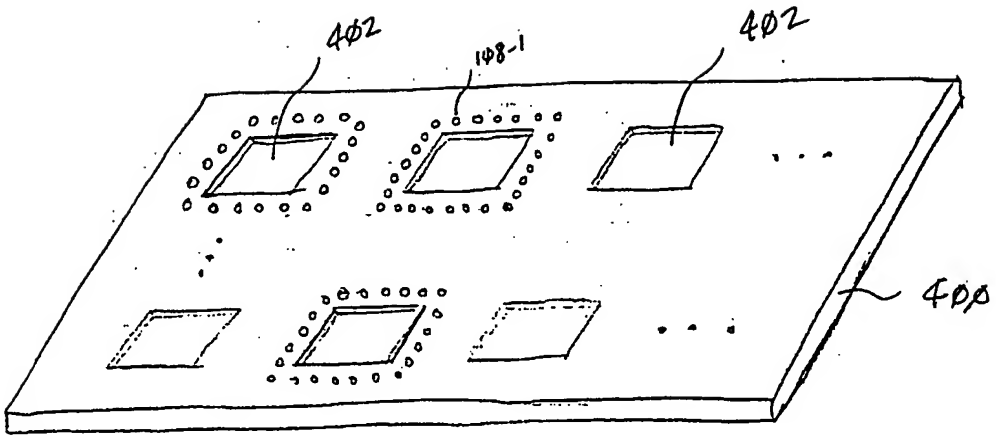
- FIGURE 1 -



- Figure 2 -



- Figure 3 -



- FIGURE 4 -

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/17721

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H01L 23/02, 23/48, 29/40, 23/52; B23K 31/02
US CL : 257/738, 778, 693, 678; 228/180.22; 438/613
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/738, 778, 693, 678; 228/180.22; 438/613

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
None

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 5-129516 A (HANABUSA ET AL.) 25 MAY 1993 (25/05/93), FIGURE 1, PAGE 85, COLUMN 1.	1, 3-6
X	US 5,578,869 A (HOFFMAN ET AL.) 26 NOVEMBER 1996 (26/11/96), FIGURE 3.	2 AND 7
A	US 5,726,489 A (MATSUDA ET AL.) 10 MARCH 1998 (10/03/98), FIGURES 5-6.	1-13
A	US 5,554,887 A (SAWAI ET AL.) 10 SEPTEMBER 1996 (10/09/96), FIGURE 2.	1-3, 7, 12, 13
A	US 5,371,404 A (JUSKEY ET AL.) 06 DECEMBER 1994 (06/12/94), FIGURES 2-3.	1-3, 7, 12, 13
A	US 5,814,894 A (IGARASHI ET AL.) 29 SEPTEMBER 1998 (29 SEPTEMBER 1998 (29/09/98), FIGURE 4.	1-3, 7, 12, 13

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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Authorized officer
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Telephone No. (703) 308-4857

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INTERNATIONAL SEARCH REPORT

International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,219,794 A (SATOH ET AL.) 15 JUNE 1993 (15/06/93), FIGURE 1.	1-7, 12, 13
A	US 5,217,922 A (AKASAKI ET AL.) 08 JUNE 1993 (08/06/93), FIGURE 1.	1-3, 7, 12, 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/17721

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/17721

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I, claim(s)1-7, 12 and 13, drawn to a semiconductor device, classified in class 257, subclass 738.

Group II, claim(s) 8-11, drawn to a method for making the semiconductor device, classified in class 438, subclass 613.

The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the device of the group I invention could be made by processes materially different from those of the group II invention, for example, instead of stamping, etching may be used.

CORRECTED VERSION*

PCT

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(81) Designated States: CN, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

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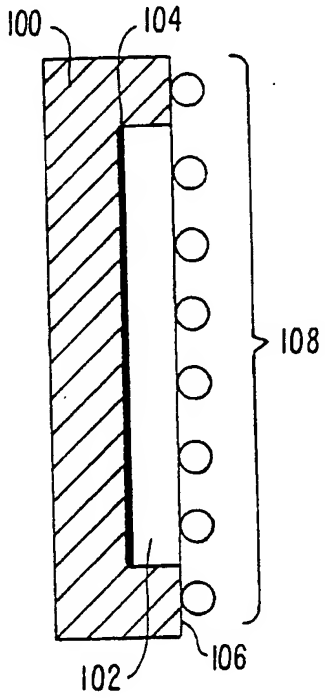
(57) Abstract

An improved semiconductor package that reduces package resistance to a negligible level, and offers superior thermal performance. A silicon die (102) is attached to a carrier (100) (or substrate) that has a cavity surrounding the die (102). Direct connection of the active surface of the silicon die (102) to the printed circuit board is then made by an array of solder bumps (108) that is distributed across the surface of the die (102) as well as the edges of the carrier (100) surrounding the die (102).



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HIGH PERFORMANCE FLIP CHIP PACKAGE

BACKGROUND OF THE INVENTION

The present invention relates in general to semiconductor packaging and in particular to an apparatus and method of manufacture for a high performance flip chip package for semiconductor devices.

While silicon process technology has advanced significantly in the past decade, for the most part, the same decades-old package technology continues as the primary packaging means. Epoxy or solder die attach along with aluminum or gold wire bonding to lead frame is still the preferred semiconductor package methodology. Advances in semiconductor processing technology, however, have made the parasitics associated with conventional packages more of a performance limiting factor. This is particularly true in the case of power switching devices where, as in the case of power MOSFETs, the on-resistance of these devices continues to push the lower limits. Thus, the parasitic resistance introduced by the bond wires and the lead frame in conventional packages becomes much more significant for such high current devices as power MOSFETs. Furthermore, the continuous shrinking of geometries and the resulting increase in chip densities has given rise to an increasing demand for semiconductor packages with lead counts higher than that offered by the conventional packaging techniques.

Ball grid array and flip chip technologies were developed to address some of these demands. Both of these packaging technologies provide for a more direct connection between the silicon die and the printed circuit board as well as providing for higher interconnect densities. There is always room for

improvement however. For example, a typical ball grid array package consists of a BT resin laminated board which serves as an interposer layer between the silicon die and the printed circuit board (PCB). Because of poor heat dissipation from the laminated board, external heat sinks and additional PCB copper layers are often required to dissipate excess heat.

In the case of conventional flip chip technology, among other shortcomings, heat dissipation is essentially governed by the die size and connection to the back side of the die is not easily facilitated (often requiring a bond wire connection). These limitations (poor heat dissipation and resistive contact to back side) become quite significant in high current applications such as power switching devices. A substantial improvement in the performance of flip chip packages is offered by Bencuya et al. in commonly assigned provisional Patent Application Number _____, (Attorney Docket No. 018865-0006) entitled "Low Resistance Package for Semiconductor Devices." In one embodiment, this improved package eliminates wire bonding by making direct connection between an array of solder balls on one conductive surface of the die and a lead frame element, while connection to the opposite side is made by a die attached mechanism. This package exhibits significantly lower resistance; however, it still relies on a lead frame which adds residual resistance to the current path, and is not the smallest package possible for a given die size.

There is therefore a need for a high density semiconductor package whose attributes are minimal parasitic resistance and good heat dissipation, and that is readily manufacturable.

SUMMARY OF THE INVENTION

The present invention provides an improved semiconductor package that reduces package resistance to a negligible level, and offers superior thermal performance. Broadly, according to the present invention, a silicon die is attached to a carrier (or substrate) that has a cavity substantially surrounding the

die. Direct connection of the active surface of the silicon die to the printed circuit board is then made by an array of solder bumps that is distributed across the surface of the die as well as the edges of the carrier surrounding the die. In one embodiment, the outer array of solder balls connects to a conductive carrier and provides for a low resistance connection to the back side of the die. In applications where no connection to the back side of the die is required, the carrier and the array of solder balls connecting to it may act as a thermal via for dissipating heat. Alternatively, the carrier may be of dielectric material with selective conductive traces to make selective contact to traces on the board through the outer array of solder balls. The package of the present invention also reduces the number of steps required in the assembly process flow and is manufactured using standard materials and equipment. The resulting package not only exhibits minimal resistance and improved heat dissipation, it is very thin and light as well as being cost-effective to manufacture.

Accordingly, in one embodiment, the present invention provides a semiconductor package including a carrier having a cavity sized for housing a silicon die, a silicon die having a first surface attached to the inside of the cavity, the silicon die having a thickness substantially equal to a depth of the cavity such that a second surface of the silicon die and a surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane, and an array of solder balls distributed across the uniform plane connecting to the second surface of the silicon die as well as the surface of the edges of the carrier surrounding the silicon die.

In another embodiment, the present invention provides a method of packaging a silicon die including the steps of: stamping a cavity in a carrier for housing the silicon die; attaching a first surface of the silicon die inside the cavity such that a second surface of the silicon die and a surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane; and disposing an array of solder balls across the substantially uniform plane with an

outer array connecting to the carrier and an inner array connecting to the second surface of the silicon die.

A better understanding of the nature and advantages of the improved flip chip package of the present invention may be gained with reference to the detailed description and drawings below.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a side view of the improved flip chip package according to the present invention;

Figure 2 illustrates the flip chip package of the present invention showing the active surface of the package with an array of solder balls;

Figure 3 shows the printed circuit board side with exemplary traces for receiving the flip chip package of the present invention; and

Figure 4 shows an exemplary embodiment for a carrier panel with multiple carriers that may be used during the process flow of the flip chip package of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figure 1, there is shown a side view of the improved flip chip package according to the present invention. A carrier 100 is provided with a rectangular cavity to receive the silicon die. A silicon wafer that has been previously back lapped and metallized to product specifications is diced and a die 102 is attached inside the cavity using any one of a variety of well known die attach methods including conductive epoxy, or soft or hard solder connection. The cavity dimensions are designed such that the cavity depth is substantially equal to the thickness of die 102 plus the thickness of die attach bond line 104. This ensures that the outer surface of die 102 and the edge surface 106 of carrier

100 surrounding die 102 form a uniform plane. Solder paste is dispensed on the surface of die 102 as well as the carrier edge surface 106. The solder paste is then reflowed using conventional methodology to form solder balls 108. Alternatively, either die 102 or carrier surfaces 106, or both can be already solder bumped prior to the die attach step. Finally, the edges of die 102 may be sealed using, for example, a conventional liquid glob top epoxy. This results in a highly compact package that is light and thin. A typical silicon die may be, for example, 0.008 inches thick and the thickness of carrier 100 at the bottom of the cavity may be, for example, 0.008 inches. This results in an exemplary package that is only 0.4 millimeter in thickness (and about 0.6 millimeter with solder balls).

The flip chip package of the present invention is particularly well suited for discrete products with high heat dissipation such as power switching devices (e.g., power MOSFETs) where electrical connection to the back side of the die (MOSFET drain terminal) is required. By using conductive material such as copper for carrier 100, the package of the present invention provides for a very low resistance, compact connection between the back side of the die (the drain terminal of the power MOSFET) and the PCB. Figure 2 is a top view of the active surface of the package of the present invention showing the array of solder balls 108. The same reference numerals denote identical elements in all of the Figures. Solder ball array 108 is divided into two groups, a first outer array of solder balls 108-1 that connects to carrier edge surface 106 and an internal array of solder balls 108-2 connecting to the die surface. When housing a power MOSFET, solder balls 108-1 provide the connection to the drain terminal, and solder balls 108-2 provide the connection to the source and gate terminals. In the embodiment shown in Figure 2, a corner solder ball 108-2G is dedicated for the gate terminal and the remaining solder balls in array 108-2 provide for a distributed, low resistance connection to the source terminal of the MOSFET. The combination of a highly conductive carrier 100 and array of solder balls 108-1 plus a distributed array of solder balls 108-2 across the surface

of the die virtually eliminate the metal resistance by drastically reducing the length of the current path through the metal connections. Figure 3 shows the printed circuit board side with exemplary traces for receiving the flip chip package shown in Figure 2.

It is to be understood that a conductive carrier for power MOSFET applications is used herein for illustrative purposes only, and that carrier 100 may be made of dielectric material such as ceramic for various other applications. Selective contact to the back side of the die is still possible with selective conductive traces through the ceramic carrier. In cases where no contact to the back side of the die is required, a metal carrier that makes no electrical contact to the die can still be used along with solder ball array 108-1 (that may be shorted together) to form a thermal via. This provides a very efficient mechanism for dissipating heat.

Another significant advantage of the improved flip chip package of the present invention is that it not only does not introduce any steps that deviate from industry standard practices, it eliminates various steps and simplifies the process of manufacture. Because the process of manufacture for the package of the present invention follows existing standards in the industry (e.g., fine pitch ball grid array standards), the tools and infrastructure necessary to support the package such as sockets, handlers, trays and the like are well established. In terms of simplification of the process of manufacture, the entire assembly process flow for the package of the present invention is reduced to the following steps: 1) wafer saw; 2) die attach and solder ball attach; 3) third optical; 4) encapsulate; 5) test; 6) singulate; and 7) tape and reel. This eliminates the need for costly mold, trim and form equipment and a plating line. Other ball count variations of the package can be easily tooled up with an initial investment in a carrier rather than dedicated items like mold, trim and form tooling that are needed for conventional surface mount packages. This improves time to market for new form factor packages.

Due to its relatively simple structure, a panel of carriers that receives the silicon dies is less costly compared to lead frames with intricate traces as required by conventional packaging. An exemplary panel 400 of carriers is shown in Figure 4. Panel 400 is made of the carrier material (e.g., copper or ceramic depending on the application) with an array of identical cavities 402 stamped across its surface the dimensions of which are governed by that of the die they will house. In one embodiment, panel 400 may include the outer array of solder balls (108-1 in Figure 2) already attached around each cavity 402 as shown. Alternatively, solder balls (108-1) may be attached later during the assembly process flow. The carriers may be tested while in a panel form and marked. The units are then individually singulated by sawing and shipped using conventional packing methods.

Thus, the present invention provides a high performance flip chip type package that offers a number of advantages over existing packaging techniques. The combination of a die attached inside a cavity of a carrier such that an array of solder balls can be disposed across both surfaces results in a highly compact, low resistance package with a simplified and thus cost effective method manufacture. The package also improves heat dissipation when the carrier is made of a highly conductive material acting as a thermal via. While the above is a complete description of the preferred embodiment of the present invention, it is possible to use various alternatives, modifications and equivalents. Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claims, along with their full scope of equivalents.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a carrier having a cavity sized for housing a silicon die;

a silicon die having a first surface attached to the inside of the cavity, the silicon die having a thickness substantially equal to a depth of the cavity such that a second surface of the silicon die and a surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane; and

an array of solder balls distributed across the uniform plane and divided into an inner array connecting to the second surface of the silicon die an outer array connecting to the surface of the edges of the carrier surrounding the silicon die.

2. The semiconductor package of claim 1 wherein the carrier is made of electrically conductive material.

3. The semiconductor package of claim 2 wherein the carrier makes electrical contact with the first surface of the silicon die.

4. The semiconductor package of claim 3 wherein the silicon die comprises a power MOSFET having a drain terminal, a source terminal, and a gate terminal.

5. The semiconductor package of claim 4 wherein the drain terminal of the power MOSFET connects to the carrier and the outer array of solder balls, the source terminal of the power MOSFET connects to a substantial number of the inner array of solder balls, and the gate terminal of the power MOSFET connects to one of the inner array of solder balls.

6. The semiconductor package of claim 2 wherein the carrier and the outer array of solder balls are configured to act as a thermal via.

7. The semiconductor package of claim 1 wherein the carrier is made of dielectric material.

8. A method for packaging a silicon die comprising the steps of:

stamping a cavity in a carrier for housing the silicon die;

attaching a first surface of the silicon die inside the cavity such that a second surface of the silicon die and a surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane; and

disposing an array of solder balls across the substantially uniform plane with an outer array connecting to the carrier and an inner array connecting to the second surface of the silicon die.

9. The method for packaging a silicon die as in claim 8 wherein said carrier is in a panel form and said step of stamping stamps a plurality of cavities across the panel.

10. The method for packaging a silicon die as in claim 9 further comprising the step of singulating the panel into plural units.

11. The method for packaging a silicon die as in claim 8 wherein the step of disposing an array of solder balls occurs prior to the attaching step and comprises a step of forming solder balls on the second surface of the silicon die, and a step of forming solder balls on the surface of the edges of the carrier.

12. A package for a silicon die comprising a power MOSFET with a source terminal, a drain terminal and a gate terminal, the package comprising:

a conductive carrier having a cavity sized for housing the silicon die such that when the silicon die is attached to the inside of the cavity an outer surface of the silicon die and the surface of the edges of the carrier surrounding the silicon die form a substantially uniform plane;

a first array of solder balls disposed across the outer surface of the silicon and making contact to the source terminal of the power MOSFET; and

a second array of solder balls disposed across the surface of the edges of the carrier surrounding the silicon die and making contact to the drain terminal of the power MOSFET through the conductive carrier.

13. The package of claim 12 wherein a solder ball on the outer surface of the silicon die makes contact to the gate terminal of the power MOSFET.

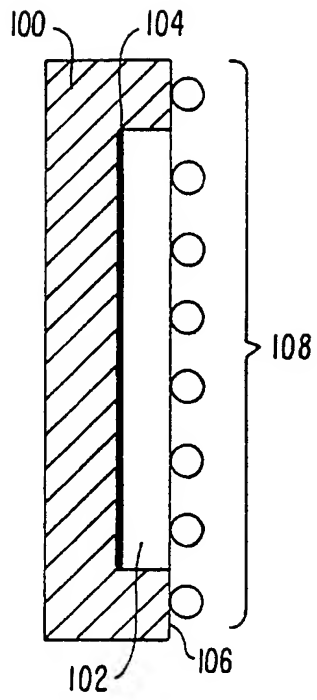

FIG. 1.

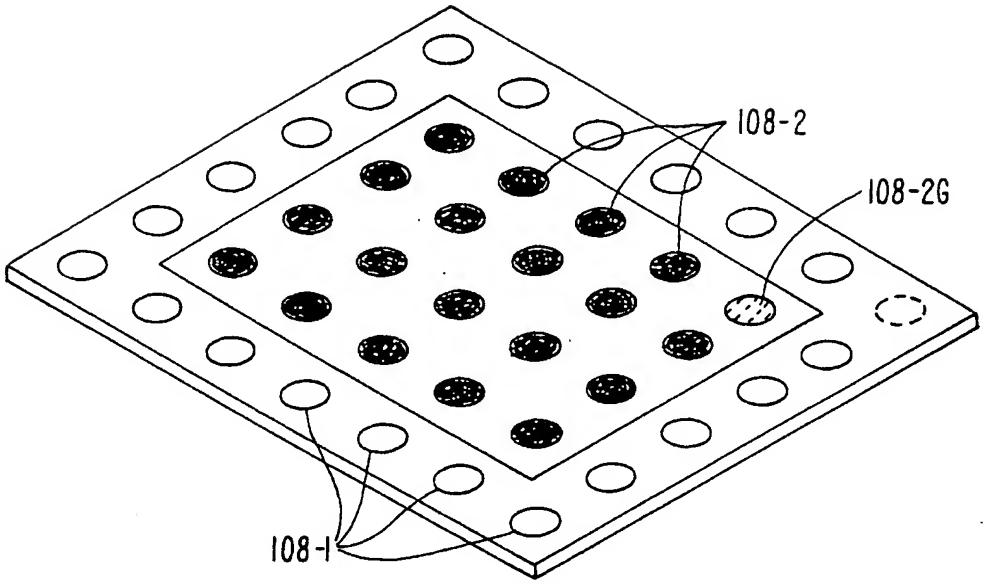
108-2
108-2G
108-1

FIG. 2.

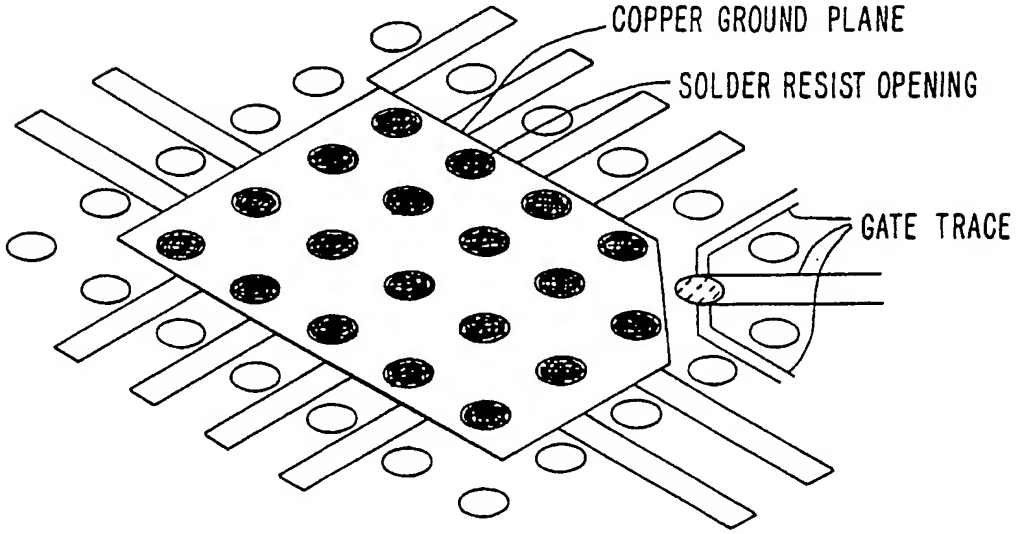
COPPER GROUND PLANE
SOLDER RESIST OPENING
GATE TRACE

FIG. 3.

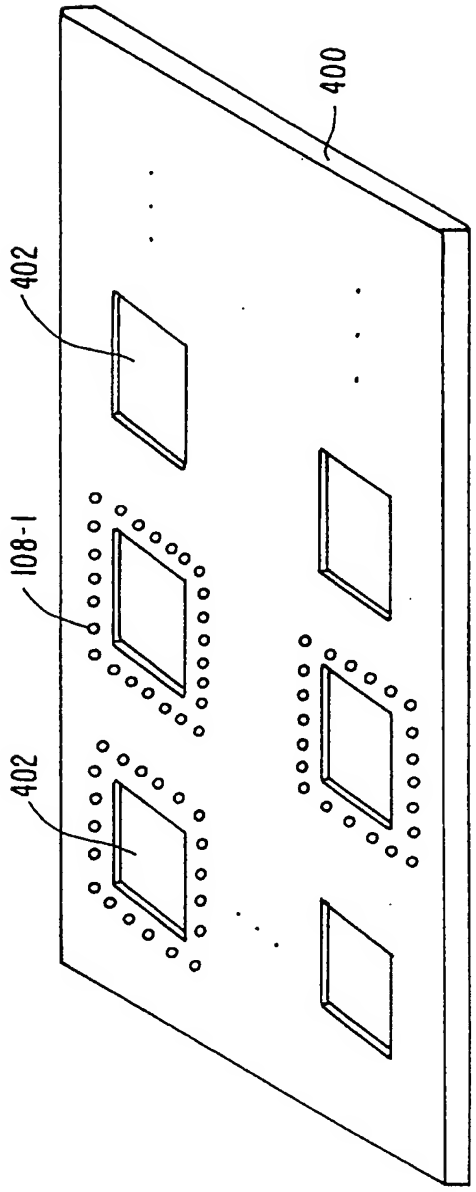

FIG. 4.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/17721

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H01L 23/02, 23/48, 29/40, 23/52; B23K 31/02
US CL : 257/738, 778, 693, 678; 228/180.22; 438/613
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/738, 778, 693, 678; 228/180.22; 438/613

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

None

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 5-129516 A (HANABUSA ET AL.) 25 MAY 1993 (25/05/93), FIGURE 1, PAGE 85, COLUMN 1.	1, 3-6
X	US 5,578,869 A (HOFFMAN ET AL.) 26 NOVEMBER 1996 (26/11/96), FIGURE 3.	2 AND 7
A	US 5,726,489 A (MATSUDA ET AL.) 10 MARCH 1998 (10/03/98), FIGURES 5-6.	1-13
A	US 5,554,887 A (SAWAI ET AL.) 10 SEPTEMBER 1996 (10/09/96), FIGURE 2.	1-3, 7, 12, 13
A	US 5,371,404 A (JUSKEY ET AL.) 06 DECEMBER 1994 (06/12/94), FIGURES 2-3.	1-3, 7, 12, 13
A	US 5,814,894 A (IGARASHI ET AL.) 29 SEPTEMBER 1998 (29 SEPTEMBER 1998 (29/09/98), FIGURE 4.	1-3, 7, 12, 13

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
02 SEPTEMBER 1999

Date of mailing of the international search report
21 OCT 1999

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231
Facsimile No. (703) 305-3230

Authorized officer
JHIHAN B. CLARK
Telephone No. (703) 308-4857

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/17721

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,219,794 A (SATOH ET AL.) 15 JUNE 1993 (15/06/93), FIGURE 1.	1-7, 12, 13
A	US 5,217,922 A (AKASAKI ET AL.) 08 JUNE 1993 (08/06/93), FIGURE 1.	1-3, 7, 12, 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/17721

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/17721

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I, claim(s)1-7, 12 and 13, drawn to a semiconductor device, classified in class 257, subclass 738.

Group II, claim(s) 8-11, drawn to a method for making the semiconductor device, classified in class 438, subclass 613.

The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the device of the group I invention could be made by processes materially different from those of the group II invention, for example, instead of stamping, etching may be used.

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